ABSTRACT

This invention is a new CMOS voltage booster (20) having an output which can be used in memories to boost the word line voltage above VDD or other voltage boosting applications. The CMOS booster includes a NMOS FET (MN1) to charge a boosting capacitor (C1) to VDD at the end of each memory access and includes a PMOS FET (MP1, MP2) to keep the voltage at the output at VDD during standby. By using this combination, the word line rise time, the size of the booster, and the power consumption during access are significantly reduced. The gate of the NMOS FET (MN1) is boosted above VDD + Vthn by a small capacitor (C2) to charge the word line boosting capacitor to VDD at the end of each memory access. The small capacitor (C2) is pre-charged to VDD by a NMOSFET (MN2) whose gate is connected to the word line boosting capacitor. The gate of each PMOS FET (MP1, MP2) is shorted to ists source to turn if off during boostenig. Ttransistor (MP3) facilitates boosting the NMOS FET (MN1) above VDD.